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Title: Method And Apparatus For Test And Characterization Of Semiconductor Components Applicants: Ware et al. Docket: RAMB-01033US1

Appl. No.: Unknown Atty: Kirk J. DeNiro, Esq.
Filing Date: January 30, 2004 Phone: (415) 369-9660

Express Mail No.: EV 332013406 US IREF RREF CLKRREF CLKTREF interconnect termination control 134b RREF 100 <u>106</u> component A 134a- $\stackrel{\mathsf{z}}{>}$ 104 $V_{\rm P}$ 102 receiver transmitter 120 132 CLK_{TA} T A R_A clock aligner clock aligner IoL current transmit receive control REF, to other circuits → from other circuits -

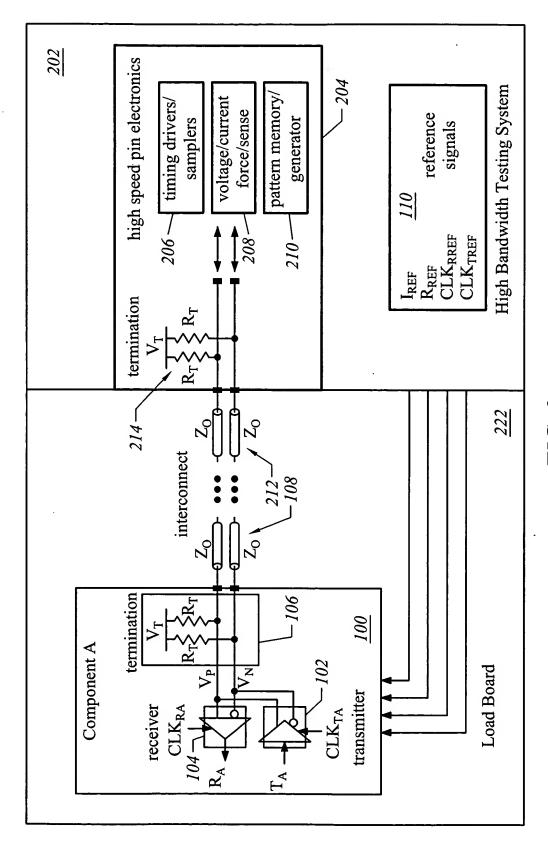
FIG. 1

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Appl. No.: Unknown Atty: Kirk J. DeNiro, Esq.
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Appl. No.: Unknown Atty: Kirk J. DeNiro, Esq.

Filing Date: Mail No. EV 332013406 HS Filing Date: January 30, 2004 Express Mail No.: EV 332013406 US 468 reference signals .466 VREF'
IREF'
RREF'
CLKRREF (See Fig. 4B) 408 transmitter A1 - under test - Z_0 V_{REF} I_{REF} R_{REF} CLK_{RREF} CLK_{TREF} termination control RREF $R_{
m T}$ 40641-'OL,T transmitter Component V_{OL,T} $V_{OH,T}$ 402 CLK_{TA} 316 314 312 420-318-40041 IA clock aligner -440AI IoL current transmit mux control generator pattern memory 327 **IREF** MON

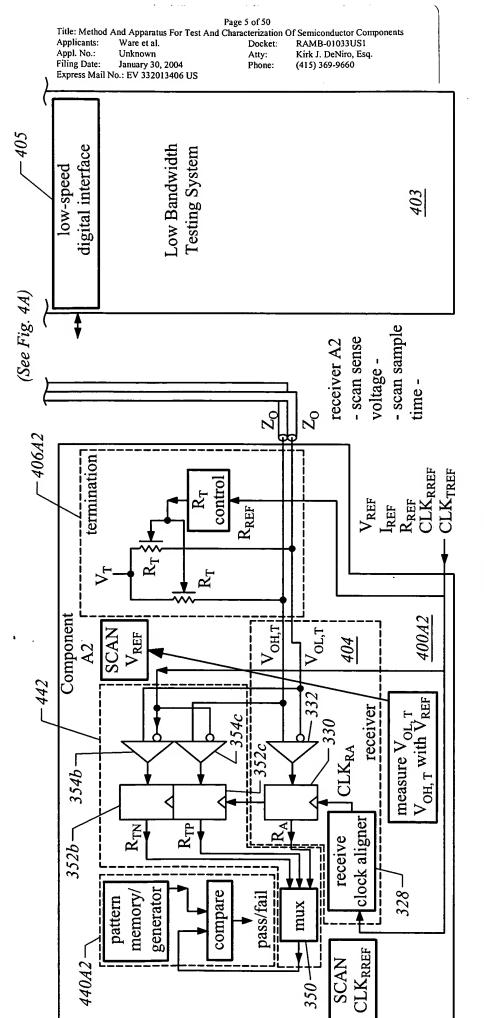
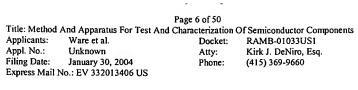
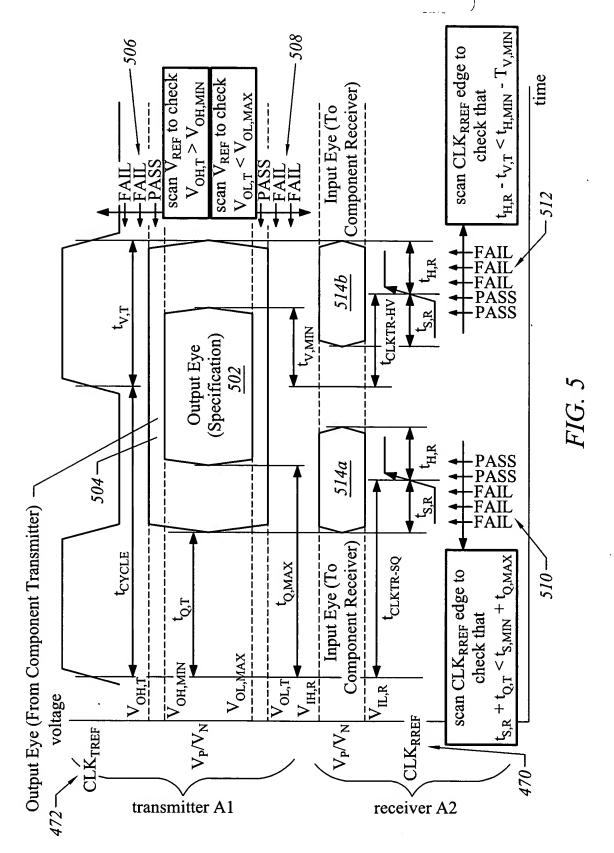
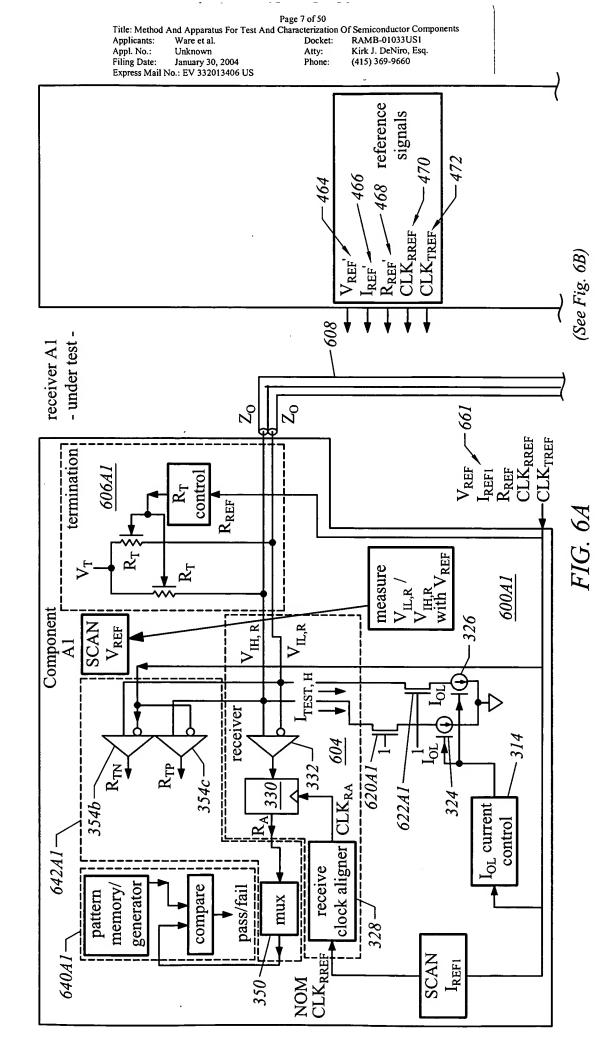


FIG. 4B







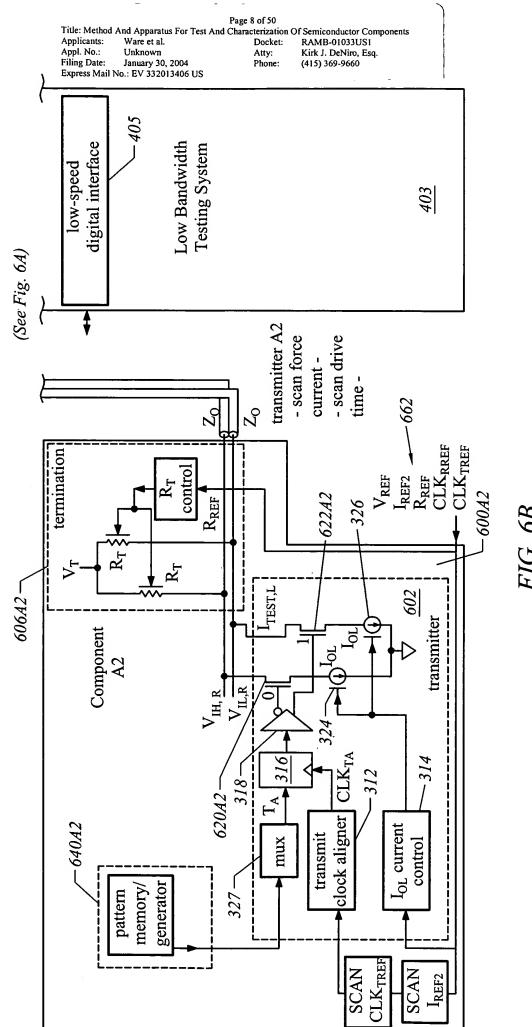


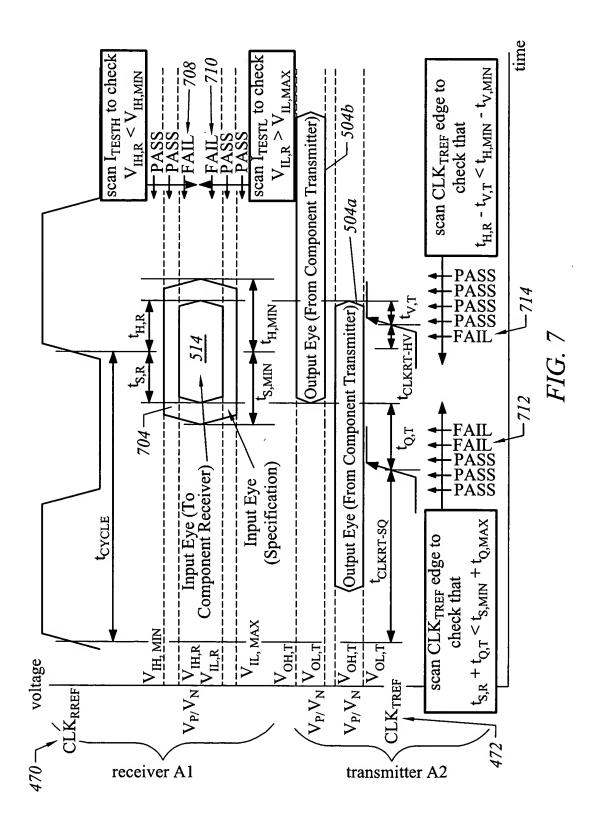
FIG. 6B

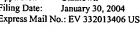
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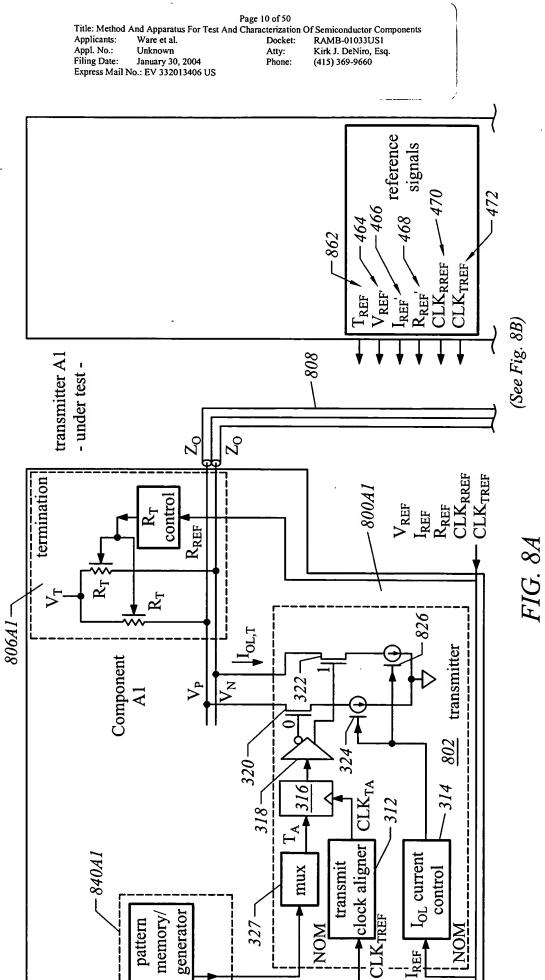
Title: Method And Apparatus For Test And Characterization Of Semiconductor Components Applicants: Ware et al. Docket: RAMB-01033US1

Applicants: Appl. No.: Filing Date: Unknown Filing Date: January 30, 2004 Express Mail No.: EV 332013406 US

Kirk J. DeNiro, Esq. Atty: (415) 369-9660 Phone:







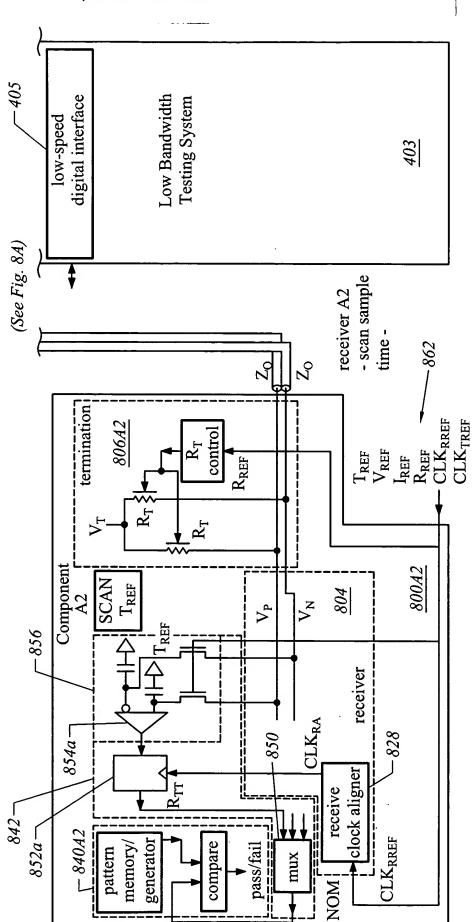
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Applicants: Appl. No.: Unknown

Docket: Atty: Phone:

RAMB-01033US1 Kirk J. DeNiro, Esq. (415) 369-9660

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scan TREF

 $V_{P'}/V_{N'}$

receiver A2 - t_Q Test

TREF

862

 $f_{S,R'} + f_{Q,T} < f_{Q,MAX}$

862

 $V_{P'}/V_{N'}$

receiver A2 - t_V Test

TREF

CLKRREF

check that edge to

CLKRREF

tQT

transmitter A1

 V_P/V_N

voltage

time

906-

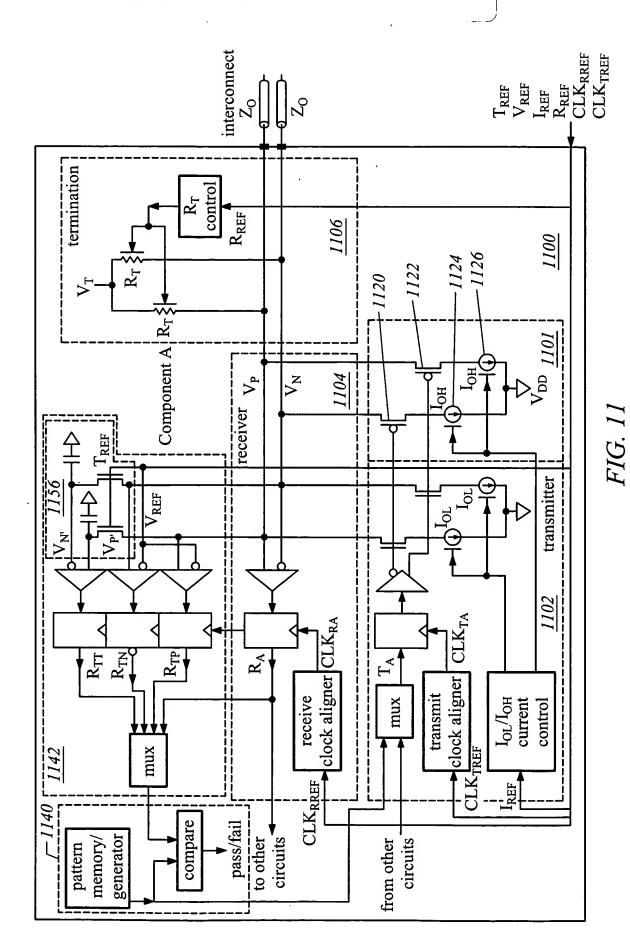
ts,r/

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Applicants: Ware et al. Docket: RAMB-01033US1 Applicants: Ware et al.
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Express Mail No.: EV 332013406 US Kirk J. DeNiro, Esq. Atty: Phone: (415) 369-9660 hold sampled $V_{P'}/V_{N'}$ on capacitors Component Transmitter) time Output Eye (From -FAIL -FAIL -FAIL -PASS -PASS Output Eye (Specification) ^LH,R 004b- 100I Input Eye (To R_T Receiver) scan t_{CLKTR-H} edge to $t_{H,R'} + t_{V,R'} < t_{H,MIN}$ Input Eye (To R_T Receiver) check that -1101 t_{v,T} teycle LV,MIN PASS PASS PASS FAIL 1004a S,R t Q,R' scan t_{CLKTR}-s 9001 check that $f_{S,R} + f_{Q,R}$ edge to tclktr-s **t**CYCLE t Q,MAX Ç trref-SH CLKTR-H voltage CLKRREF V_P/V_N $V_{p'}/V_{N'}$ I'REF receiver A2 - t_S Test transmitter A1 receiver A2 - t_H Test

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Express Mail No.: EV 332013406 US



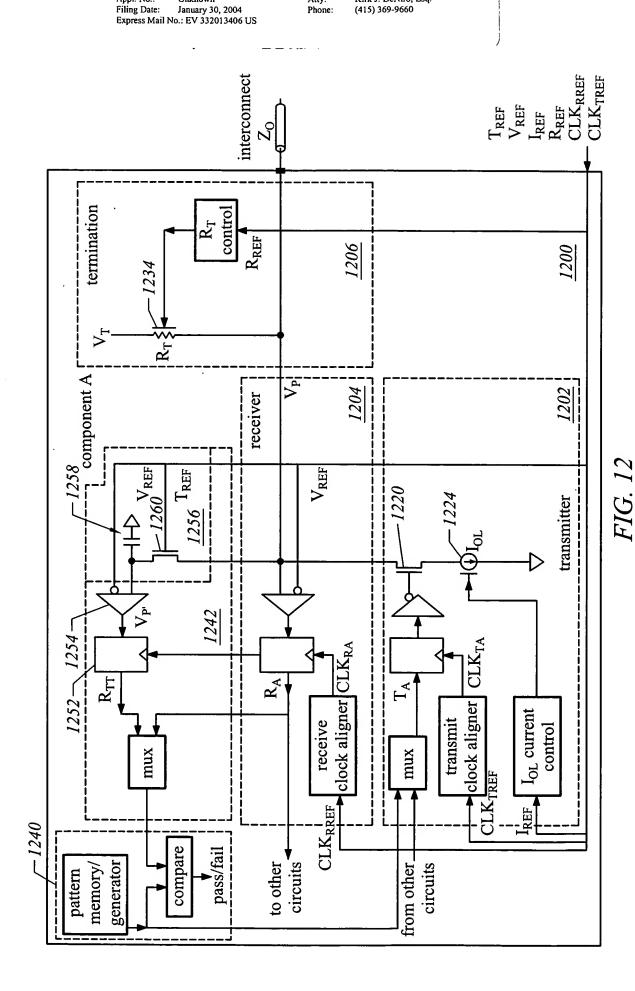
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Express Mail No.: EV 332013406 US

Docket: RAMB-01033US1 Atty: Kirk J. DeNiro, Esq. Phone: (415) 369-9660

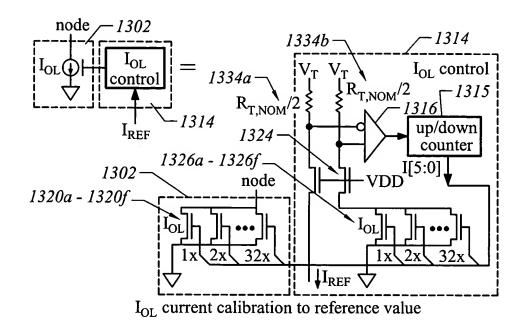
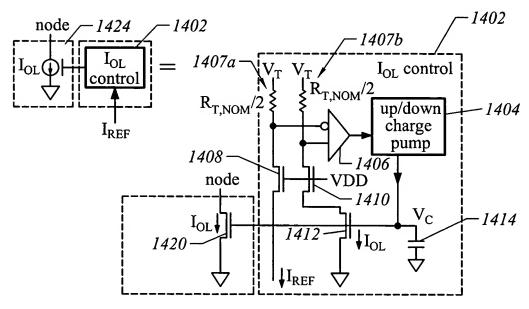


FIG. 13



I_{OL} current calibration to reference value with analog control voltage

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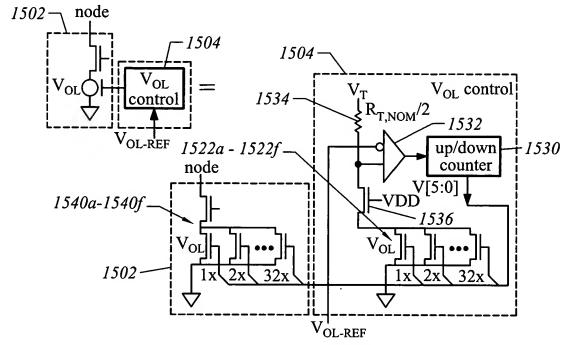
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Appl. No.: Unknown Atty: Kirk J. DeNiro, Esq.

Applicants: Appl. No.: Filing Date: Filing Date: January 30, 2004 Express Mail No.: EV 332013406 US

Atty: Phone:

Kirk J. DeNiro, Esq. (415) 369-9660



V_{OL} voltage calibration to reference value

FIG. 15

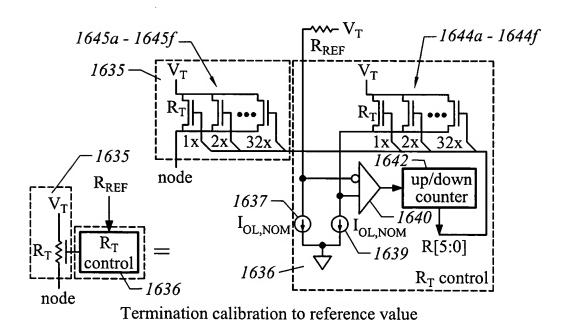
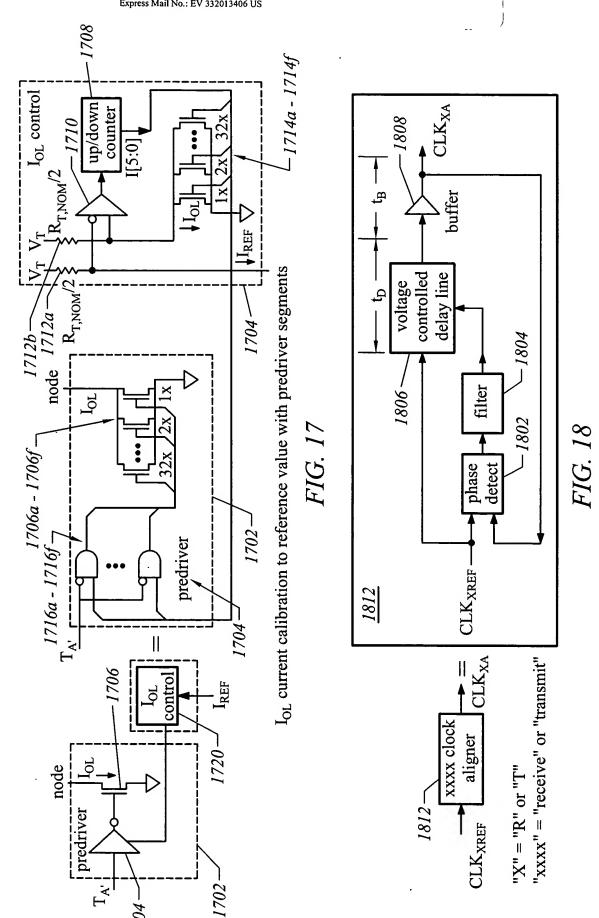


FIG. 16

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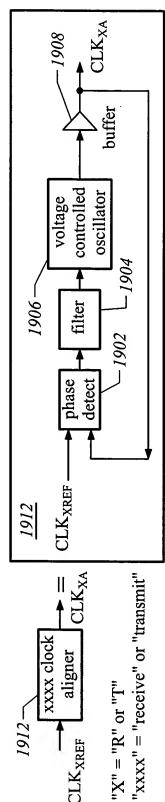
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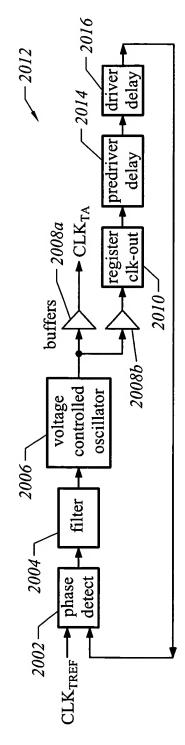
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Applicants: Ware et al. Docket: RAMB-01033US1
Appl. No.: Unknown Atty: Kirk J. DeNiro, Esq.
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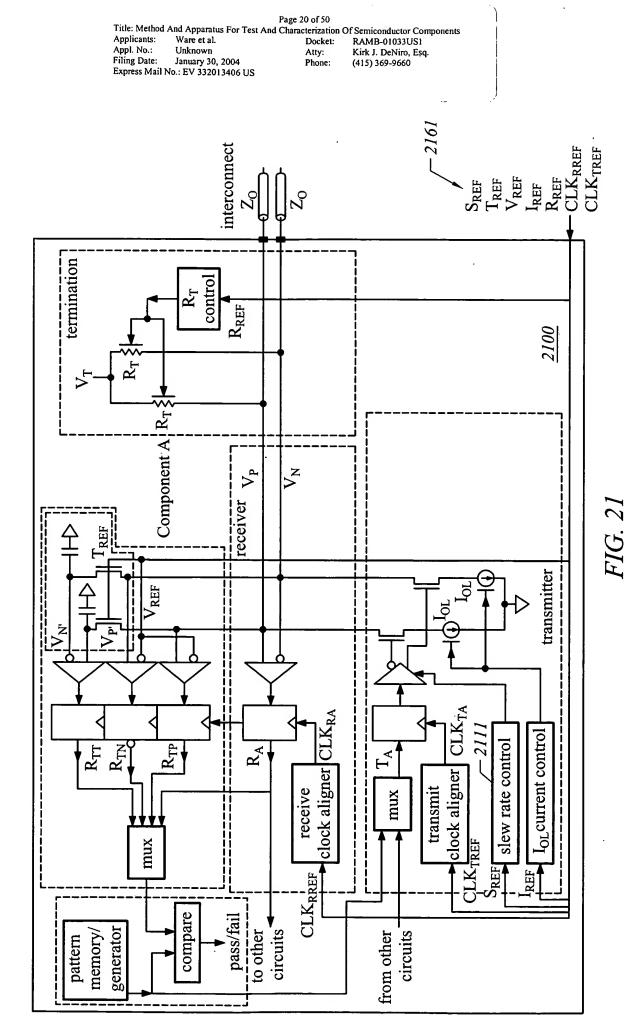
Receive or transmit clock alignment using PLL (phase-locked-loop)





Transmitter clock aligner with output register/predriver/driver loop compensation

FIG. 20



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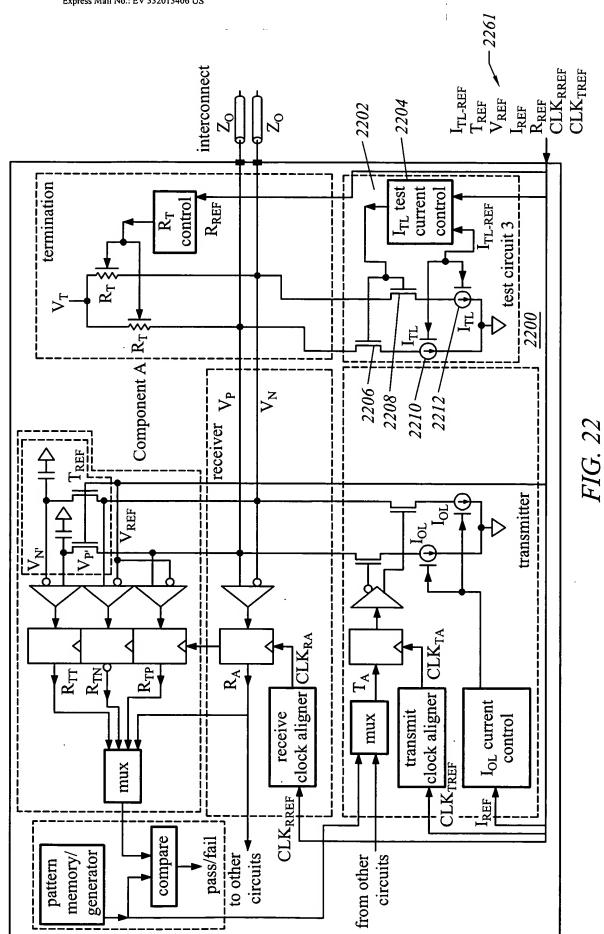
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Ware et al. Docket: RAMB-01033US1

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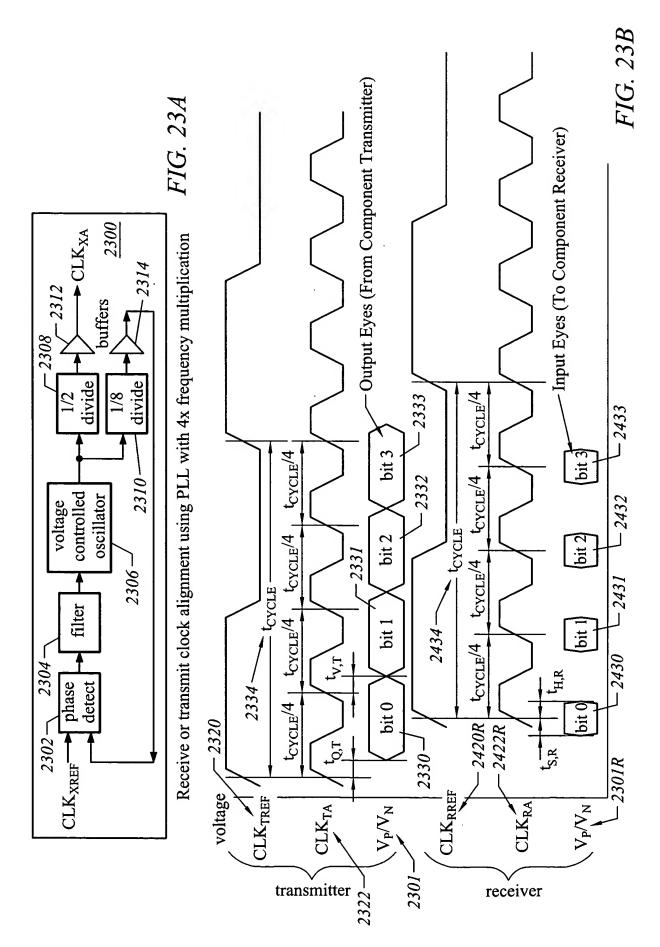
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Applicants: Ware et al. Docket: RAMB-01033US1
Appl. No.: Unknown Atty: Kirk J. DeNiro, Esq.

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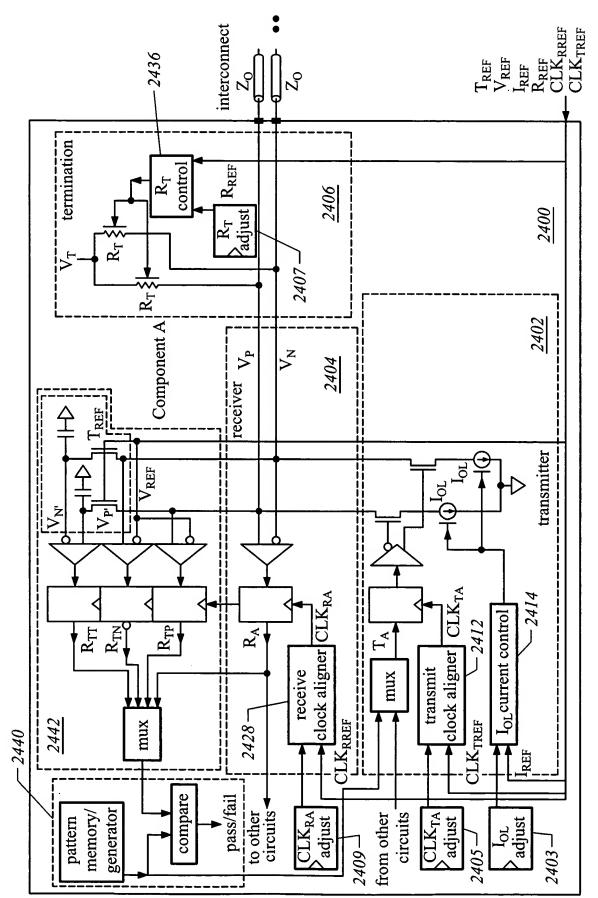


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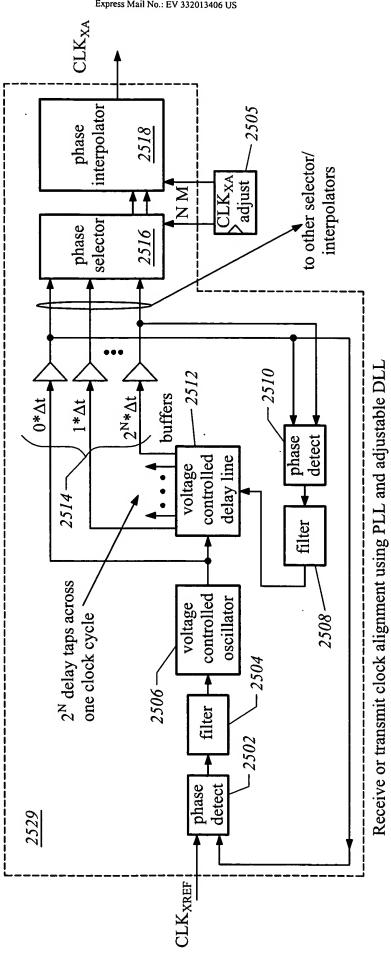


FIG. 25

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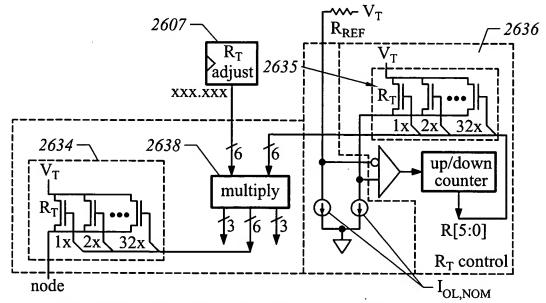
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Appl. No.: Unknown Filing Date: January 30, 2004

Atty: Phone: Kirk J. DeNiro, Esq.

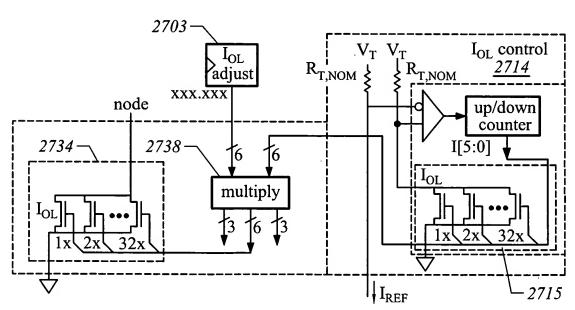
Express Mail No.: EV 332013406 US

(415) 369-9660



Adjustable termination with calibration to reference value

FIG. 26



Adjustable I_{OL} current with calibration to reference value

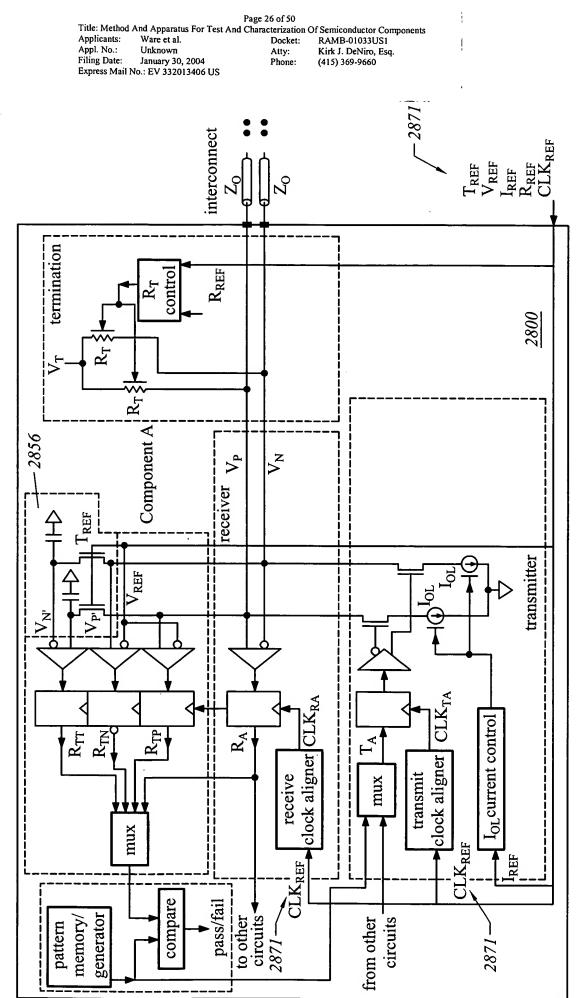
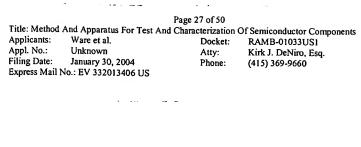
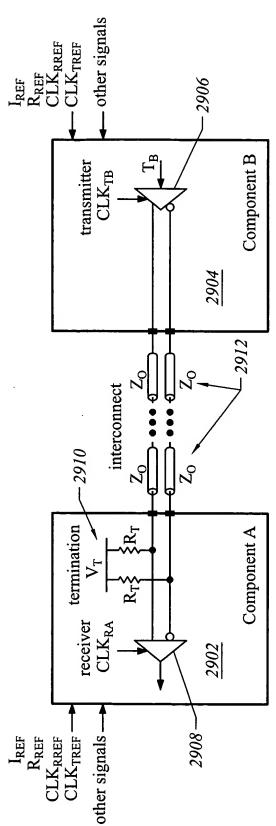


FIG. 28

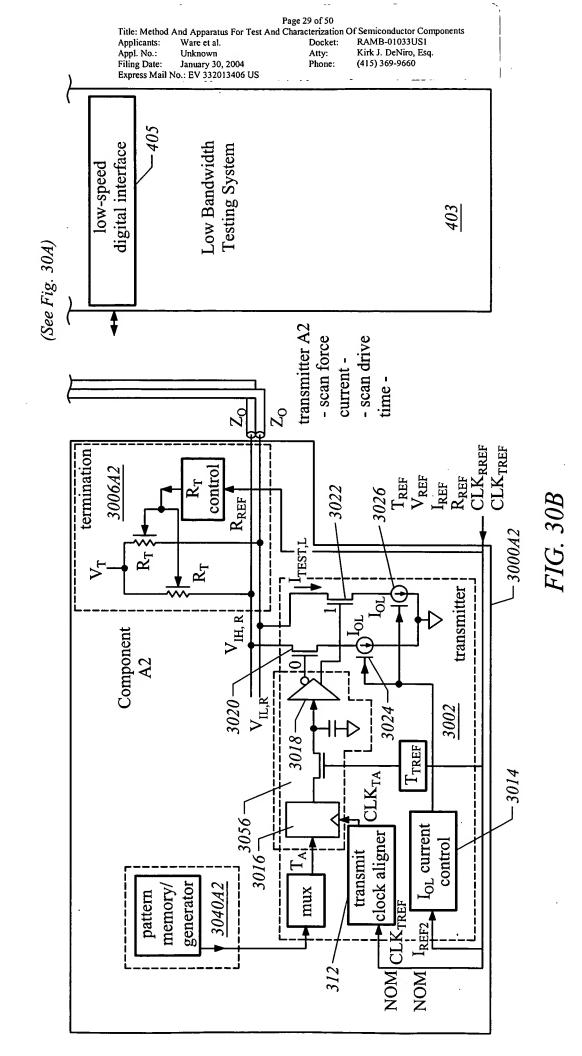




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Express Mail No.: EV 332013406 US -366 reference signals .370 -372 368 364 -362 RREF' CLKRREF. CLKTREF (See Fig. 30B) Tref Vref Iref 808 - under test receiver A1 Z_0 Zo V_{REF} IREF1 RREF CLKRREF —CLKTREF termination control FIG. 304 RREF 80642 $m R_T$ 300041 Component A1 326 V_{IL,R} ! 322 $V_{IH,R}$ 304 receiver 덛 CLKRA mux 320 340 I_{OL} current control clock aligner receive 314 generator memory/ compare pass/fail pattern NOM IREF1 CLKRREF SCAN

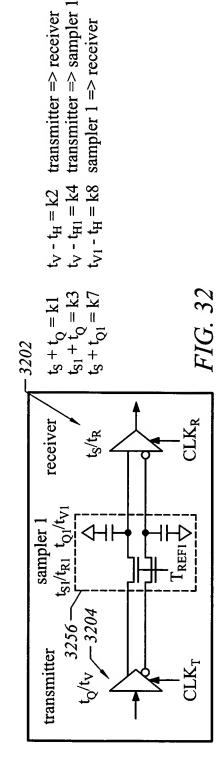


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Docket: RAMB-01033US1 Atty: Phone: Kirk J. DeNiro, Esq. (415) 369-9660

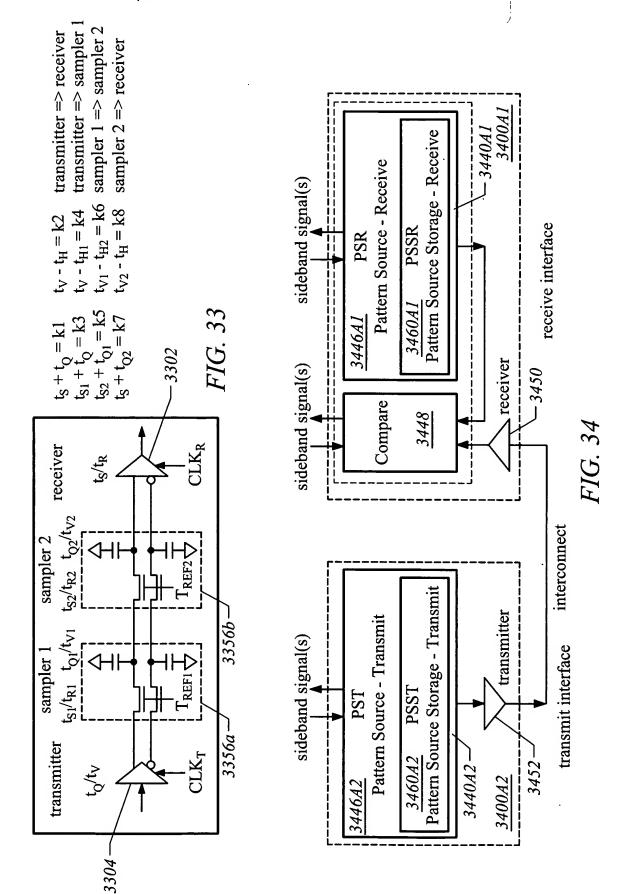
 $t_v - t_H = k2$ transmitter => receiver $t_S + t_Q = k1$ CLK_R receiver $t_{\rm s}/t_{\rm R}$ transmitter t_Q/t_V



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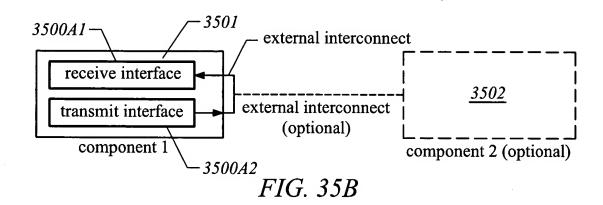


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3501 3500A1internal interconnect receive interface *3502* transmit interface external interconnect (optional) component 1 component 2 (optional) 3500A2

FIG. 35A



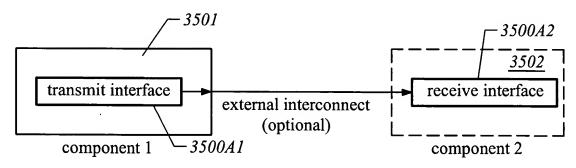


FIG. 35C

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Docket: RAMB-01033US1 Atty: Kirk J. DeNiro, Esq. Phone: (415) 369-9660

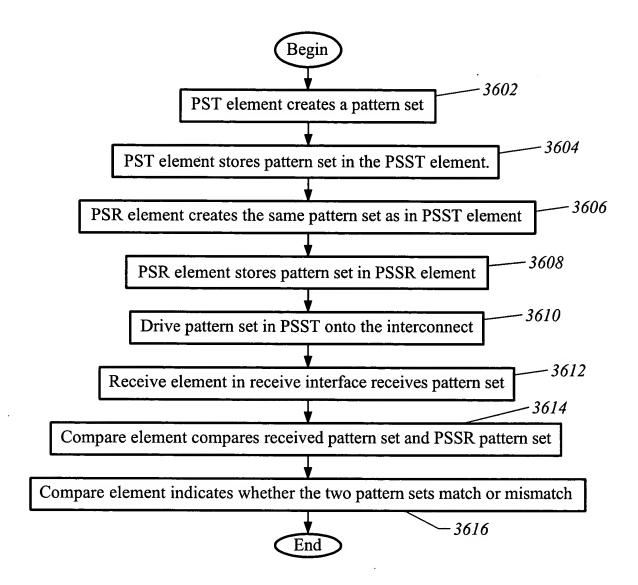
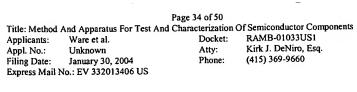


FIG. 36



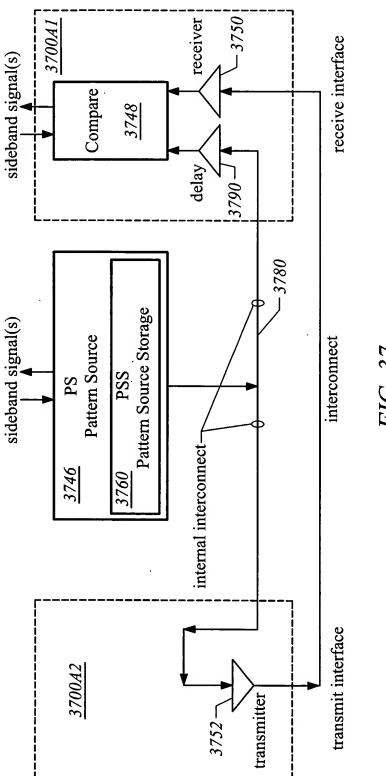
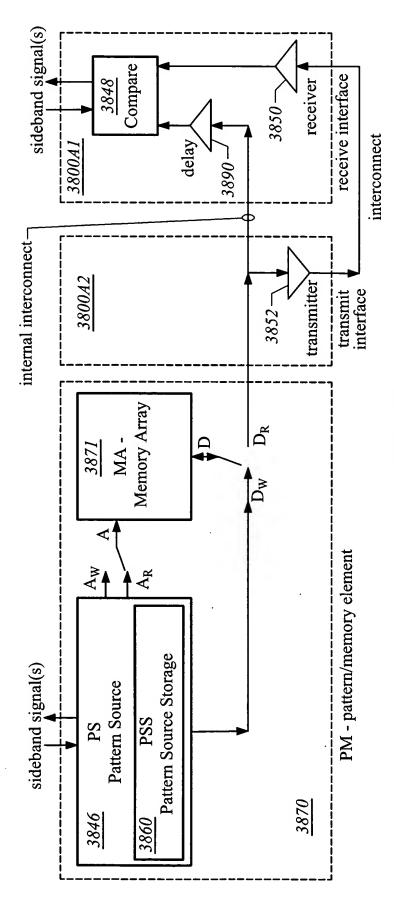


FIG. 37

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Express Mail No.: EV 332013406 US



Title: Method And Apparatus For Test And Characterization Of Semiconductor Components Applicants: Ware et al. Docket: RAMB-01033US1 Kirk J. DeNiro, Esq. Appl. No.: Unknown Atty: January 30, 2004 Filing Date: (415) 369-9660 Phone: Express Mail No.: EV 332013406 US Begin - 3902 PS element creates a pattern set 3904 -PS element stores pattern set in the PSS element. PS element generates a write address Aw and 3910 places on A port of memory array element Final 3906 pattern set written PS element drives pattern set on D_w and writes to memory array into memory array element through D port element? -3908 Yes 3914 PS element generates a read address AR and places on A port of memory array element Memory array element reads pattern set on D_R -3916 and drives pattern set to transmit interface - 3918 Transmitter drives pattern set onto interconnect 3920 Receiver reveives pattern set from interconnect 3922 Delay element receives pattern set from D_R - 3924 Compare element compares patterns sets from delay element and receiver Compare element stores match or mismatch indication 3926 3928 -Final pattern set read from memory array No element? 3932 FIG. 39 End

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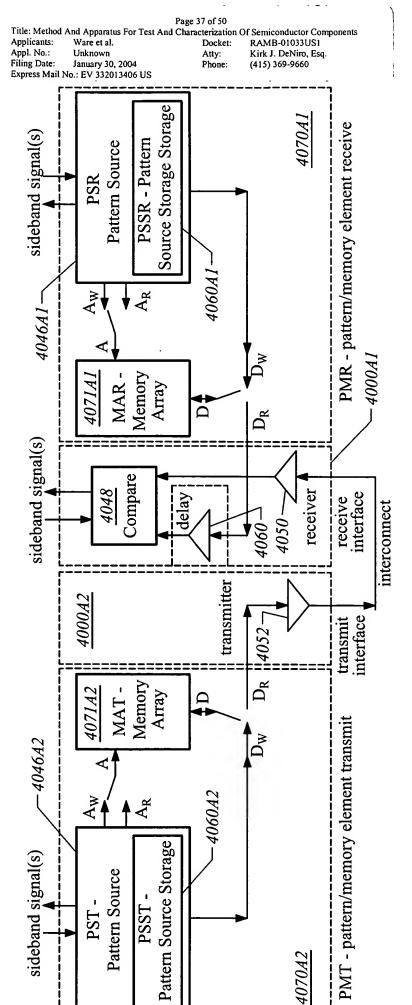
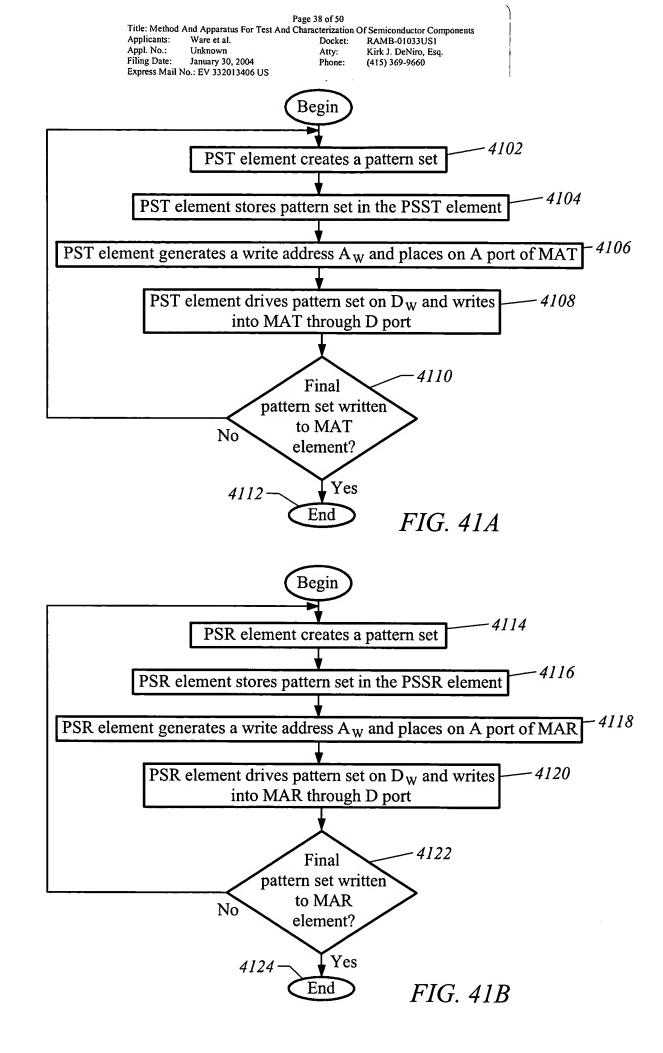


FIG. 40



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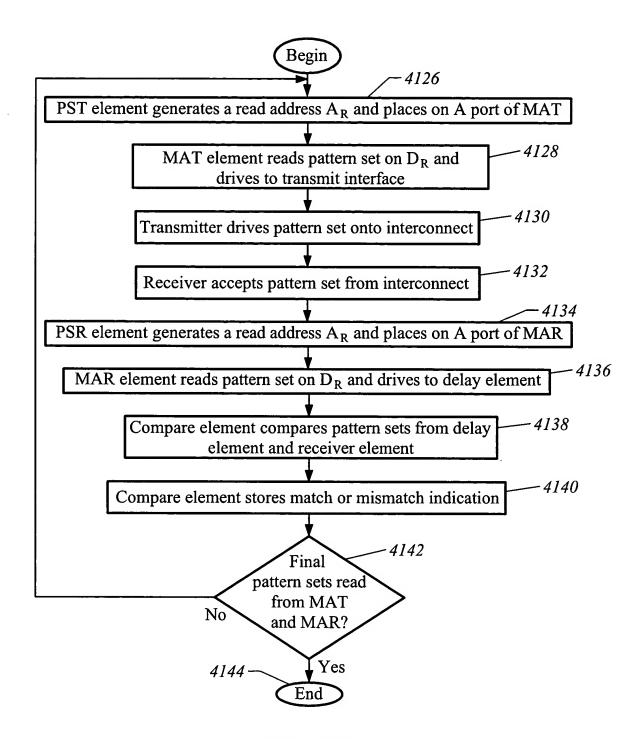


FIG. 41C

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Express Mail No.: EV 332013406 US

Docket: R
Atty: K
Phone: (4

RAMB-01033US1 Kirk J. DeNiro, Esq. (415) 369-9660

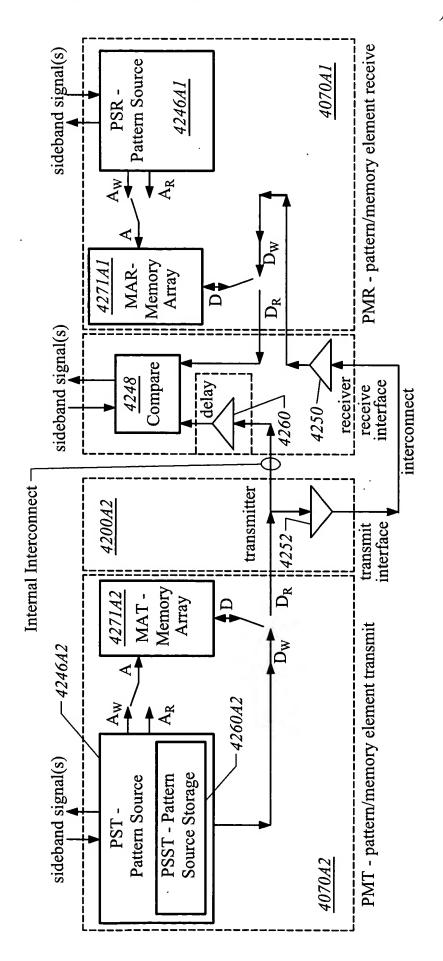


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Kirk J. DeNiro, Esq. (415) 369-9660 Atty: Phone:

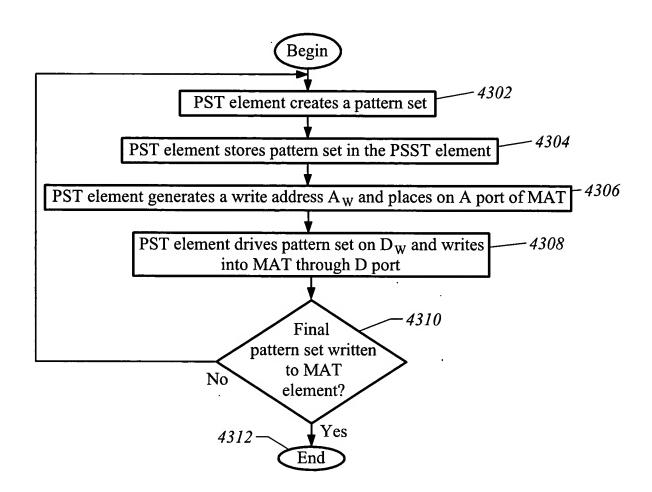


FIG. 43A

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Express Mail No.: EV 332013406 US

Atty: Kirk J. DeNiro, Esq. Phone: (415) 369-9660

ng Date: January 30, 2004 Phone: (415) 369-9660 ress Mail No.: EV 332013406 US

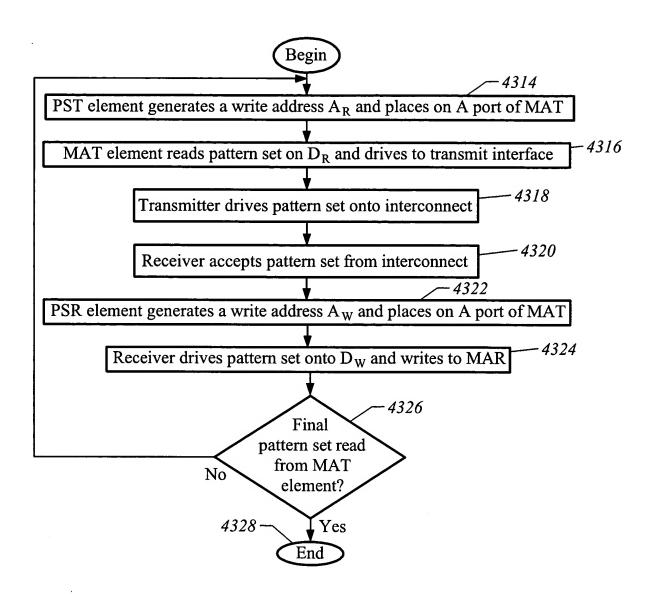


FIG. 43B

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Atty: Kirk J. Phone: (415) 3

Kirk J. DeNiro, Esq. (415) 369-9660

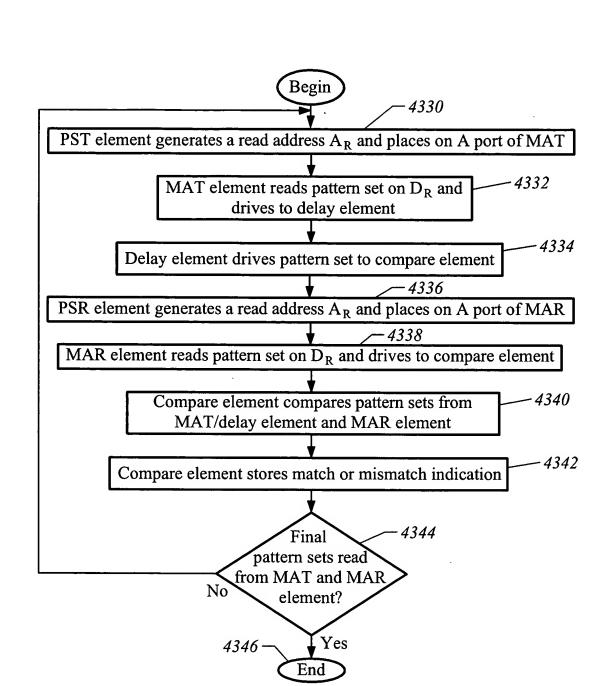


FIG. 43C

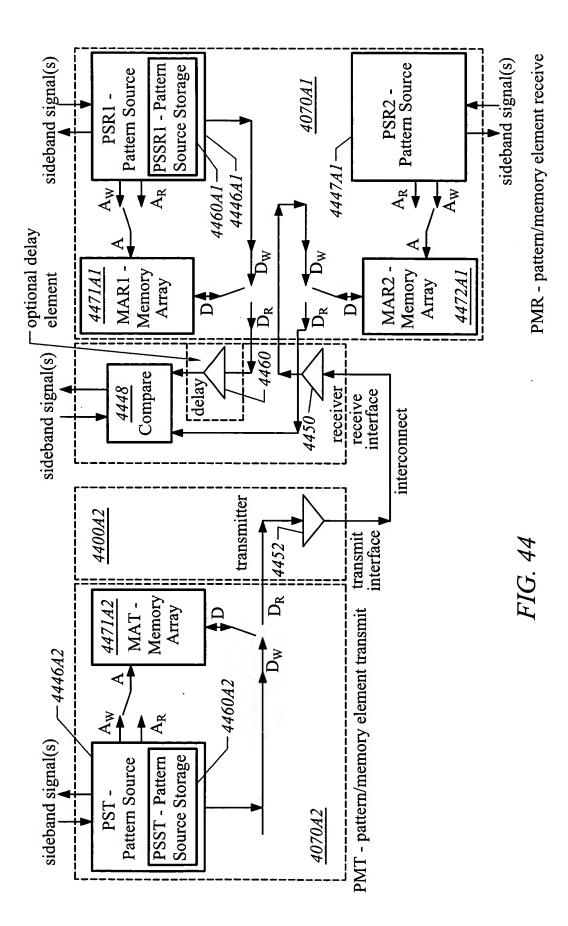
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Title: Method And Apparatus For Test And Characterization Of Semiconductor Components
Applicants: Ware et al. Docket: RAMB-01033US1
Appl. No.: Unknown Atty: Kirk J. DeNiro, Esq.

Filing Date: January 30, 2004 Express Mail No.: EV 332013406 US

Atty: Phone:

(415) 369-9660



Page 45 of 50 Title: Method And Apparatus For Test And Characterization Of Semiconductor Components Applicants: RAMB-01033US1 Ware et al. Docket: Kirk J. DeNiro, Esq. Unknown Appl. No.: Atty: Filing Date: January 30, 2004 Express Mail No.: EV 332013406 US (415) 369-9660 Phone: Begin 4502 PST element creates a pattern set - 4504 PST element stores pattern set in the PSST element 4506 PST element generates a write address Aw and places on A port of MAT PST element drives pattern set on D_w and writes -4508 into MAT through D port -4510 Final pattern set written to MAT No element? Yes 4514-End FIG. 45A Begin 4516 PSR1 element generates a pattern set -4518 PSR1 element stores pattern set in the PSSR1 element 4520 PSR1 element generates a write address Aw and places on A port of MAR1 PSR1 element drives pattern set on Dw and 4522 writes it into D port of MAR1 4524 Final pattern set written to MAR1

No

4528

element?

End

Yes

FIG. 45B

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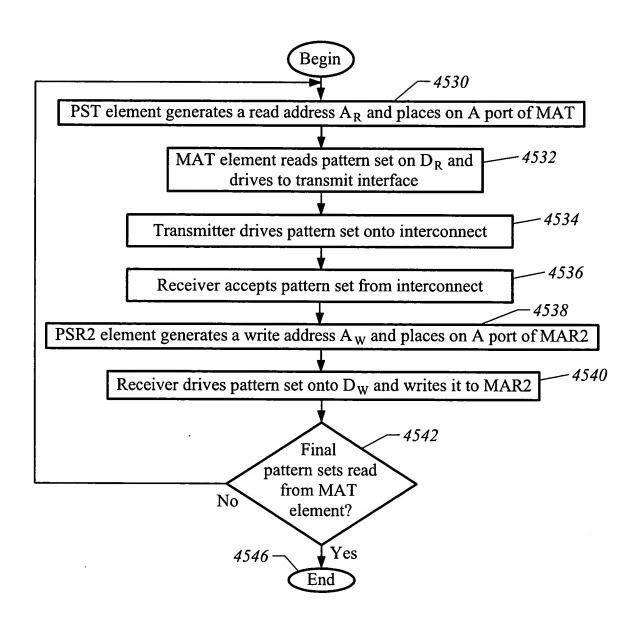


FIG. 45C

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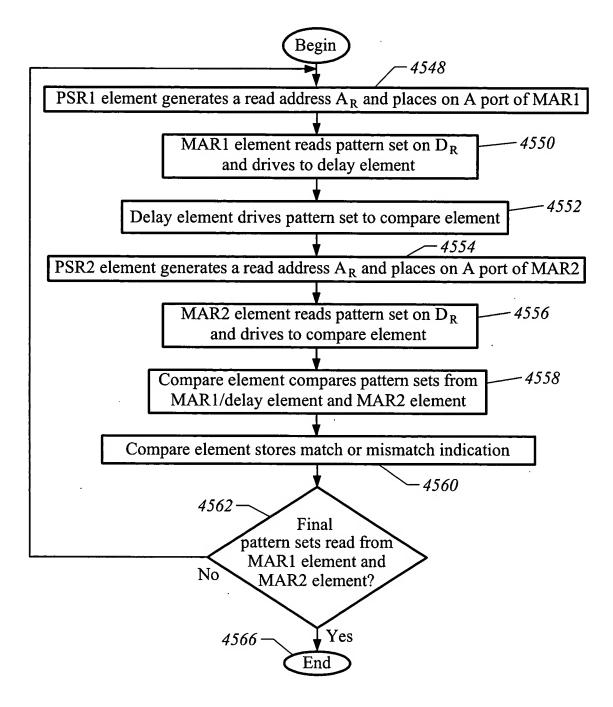


FIG. 45D

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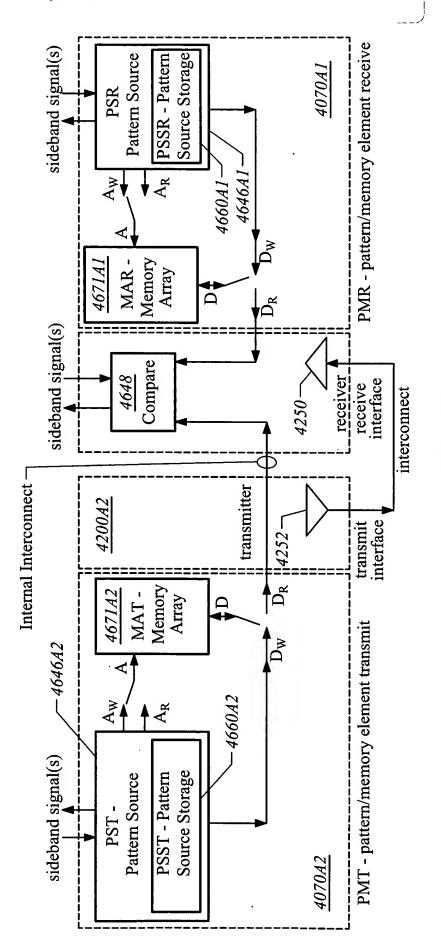


FIG. 46

Title: Method And Apparatus For Test And Characterization Of Semiconductor Components Applicants: Ware et al. Docket: RAMB-01033US1 Kirk J. DeNiro, Esq. Atty: Filing Date: January 30, 2004 (415) 369-9660 Phone: Express Mail No.: EV 332013406 US Begin 4702 PST element creates a pattern set 4704 PST element stores pattern set in the PSST element 4706 PST element generates a write address Aw and places on A port of MAT PST element drives pattern set on D_W and writes -4708 into MAT through D port 4710 Final pattern set written to MAT No element? Yes 4714 End FIG. 47A Begin 4716 PSR element creates a pattern set 4718 PSR element stores pattern set in the PSSR element PSR element generates a write address Aw and places on A port of MAR PSR element drives pattern set on Dw and 4722 writes it into MAR through D port 4724 Final pattern set written to MAR No element? . Yes 4728 End FIG. 47B

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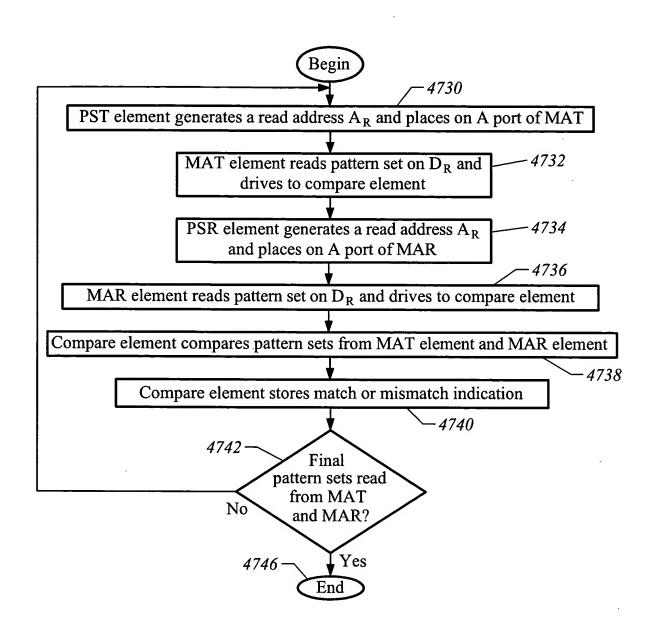


FIG. 47C